Micropatterned Single-Walled Carbon Nanotube Electrodes for Use in High-Performance Transistors and Inverters

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S *Supporting Information*

ABSTRACT: We demonstrated the solution-processed single-walled carbon nanotube (SWNT) source−drain electrodes patterned using a plasma-enhanced detachment patterning method for high-performance organic transistors and inverters. The high-resolution SWNT electrode patterning began with the formation of highly uniform SWNT thin films on a hydrophobic silanized substrate. The SWNT source−drain patterns were then formed by modulating the interfacial energies of the prepatterned elastomeric mold and the SWNT thin film using oxygen plasma. The SWNT films were subsequently selectively delaminated using a rubber mold. The patterned SWNTs could be used as the source−drain electrodes for both n-type PTCDI-C8 and p-type pentacene field-effect transistors (FETs). The n- and p-type devices exhibited good and exactly matched electrical performances, with a field-effect mobility of around 0.15 cm^2 V^{-1} s^{-1} and an ON/OFF current ratio exceeding 10^6. The single electrode material was used for both the n and p channels, permitting the successful fabrication of a high-performance complementary inverter by connecting a p-type pentacene FET to an n-type PTCDI-C8 FET. This patterning technique was simple, inexpensive, and easily scaled for the preparation of large-area electrode micropatterns for flexible microelectronic device fabrication.

KEYWORDS: *organic field-effect transistor, source−drain electrode, single-walled carbon nanotube, plasma-enhanced detachment patterning, micropattern, inverter*
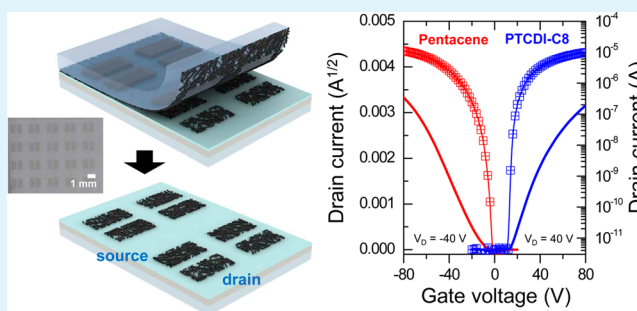
1. INTRODUCTION

Organic field-effect transistors (OFETs) have attracted considerable attention recently as a central component of low-cost flexible electronic devices.[1−5] OFET-based complementary circuits that combine n- and p-channel semiconducting materials reduce power consumption, increase operating speeds, and increase noise-tolerance margins.[6,7] The development of high-performance inverter devices depends on the availability of both n- and p-type organic semiconductors with high field-effect mobilities. Additionally, the availability of solution-processable electrode materials is crucial for achieving powerful complementary circuit technologies. For example, electrodes with high work functions are generally used in conjunction with p-type semiconductors because they present a low hole-injection barrier, whereas electrodes with low work functions are generally paired with n-type transistors to reduce the electron-injection barrier.[8,9] Two types of electrode materials are, therefore, needed for the fabrication of high-performance complementary inverters. Universal solution-processable electrode materials that are compatible with both

n- and p-type semiconductors would facilitate the processes required for fabricating high-performance inverters.

Solution-processable electrode materials have been identified for use as source−drain electrodes in OFETs.[10−13] For example, poly(3,4-ethylenedioxythiophene):poly-(styrenesulfonate) (PEDOT:PSS) conducting polymers were utilized to reduce the contact resistance at an electrode/semiconductor interface.[14−16] The conductivity of PEDOT:PSS conducting patterns, however, remains too low to be useful for the fabrication of large-area electronic circuits. Metal nanoparticles are another candidate solution-processable electrode material.[17−21] They, too, are limited in their utility because the nanoparticle sintering process for enhancing the connectivity between particles reduces their compatibility with various flexible substrates. Recently, carbon nanotubes (CNTs) have drawn significant interest as ideal electrode materials for a variety of organic devices because CNTs display a high
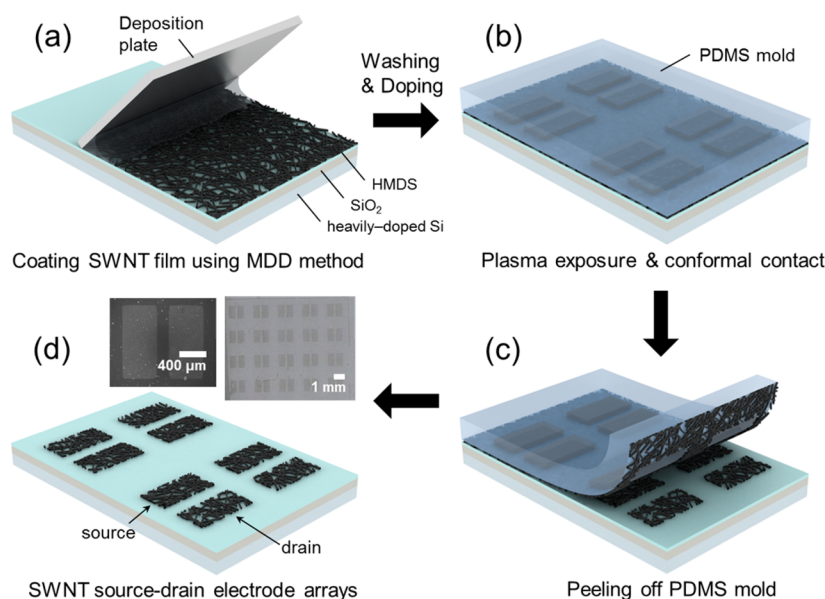
Figure 1. Schematic illustration of the fabrication of SWNT source−drain electrode patterns for high-performance OFETs. (a) Fabrication of a SWNT thin film on a HMDS-treated Si/SiO$_2$ wafer using MDD techniques. (b) After plasma exposure, conformal contact made between the SWNT film and prepatterned PDMS mold. (c) PDMS mold peeled off. (d) Micropatterned SWNT electrode arrays. The inset shows SEM and OM images of the SWNT source−drain electrode arrays prepared on the HMDS-treated Si/SiO$_2$ wafer.

conductivity, high chemical and mechanical stabilities, and a transparency that approaches that of indium−tin oxide (ITO).[22,23] The use of CNTs as electrodes requires the development of versatile patterning methods for preparing electrodes with low contact resistance and favorable charge-injection properties when paired with the organic semi-conductor layers. Patterning CNTs through solution processes has been realized by means of self-assembly,[24] micromolding in a capillary,[25] and transfer printing of CNT thin films[26−28] that were prepared by spin coating, vacuum filtration, or Langmuir−Blodgett assembly. These methods, however, have certain drawbacks. For example, the patternable shapes are limited to simple strips, an additional transfer process is necessary, and a large quantity of the CNT suspension is consumed.

In this work, we demonstrated the micropatterning of a representative carbon nanomaterial, single-walled carbon nano-tubes (SWNTs), for the preparation of high-performance transistors and inverters. Our method for patterning SWNT electrode arrays was based on the formation of highly uniform SWNT thin films directly on hydrophobic silanized substrates with a small amount of SWNT solution, modulation of the surface energies of the SWNT film, and delamination of the SWNT film using plasma-treated elastomeric molds. Our SWNT micropatterns may be used as source−drain electrodes for both n-type PTCDI-C8 and p-type pentacene field-effect transistors (FETs). The electrical performances of both devices were exactly matched, with a field-effect mobility of around 0.15 cm^2 V^{-1} s^{-1} and an ON/OFF current ratio exceeding 10^6. High-performance complementary inverters prepared with patterned SWNT electrodes were successfully demonstrated using both p-type pentacene and n-type PTCDI-C8. Our method of patterning high-resolution SWNT microstructures provides a novel approach to realizing next-generation organic electronics.

2. EXPERIMENTAL SECTION

Preparation of Aqueous SWNT Dispersions. The SWNTs synthesized by the arc discharge method were obtained from Hanwha Chemical. The SWNT dispersion (0.3 wt %) was prepared using Milli-Q water containing 1 wt % sodium dodecylbenzenesulfonate (SDBS; Sigma-Aldrich) and 3 wt % Triton X-100 (TX-100; Sigma-Aldrich). After ultrasonication, the dispersion of SWNTs was centrifuged at 13000 rpm for 30 min to remove SWNT agglomerates (WiseSpin CF-10, Daihan Scientific). The resulting homogeneous dispersion of SWNTs was mixed with 10 vol % ethylene glycol (Sigma-Aldrich) to obtain a SWNT solution with a concentration of 2.0 mg mL^{-1}.

Fabrication of OFETs with SWCNT Electrodes. The SWNT thin films were fabricated using a microliter-scale solution process, called the meniscus-dragging-deposition (MDD) technique.[29] The glass deposition plate (2.5 × 7.5 cm^2 with a plain end, Fisher Scientific) and a silicon wafer bearing a thermally grown 300-nm-thick oxide layer were cleaned in piranha solution for 30 min at 100 °C, thoroughly rinsed with copious amounts of distilled water, and dried. The wafer served as the gate electrode and the oxide layer as the gate dielectric. Hexamethyldisilazane (HMDS; Aldrich Chemical Co.) was applied to the Si/SiO$_2$ wafer using a method reported previously.[30−32] A drop of the as-prepared SWNT solution with a volume of 40 μL was introduced between the deposition plate and the HMDS-treated Si/SiO$_2$ substrate. A motorized stage (AL1-1515-3S, Micro Motion Technology) moved the deposition plate linearly in an alternating motion with a constant speed of 20 mm s^{-1} to deposit the SWNTs on the coating substrate. The resulting SWNT thin film was immersed in a 50 vol % ethanol solution at 50 °C for 1 h to wash away the surfactants and ethylene glycol. After drying, the SWNT thin film was doped with nitric acid (90%, Sigma-Aldrich) for 30 min and placed on a hot plate at 80 °C. Prepatterned elastomeric molds were fabricated by casting poly(dimethylsiloxane) (PDMS) prepolymer (Sylgard 184, Dow Corning) onto a SU-8 photoresist (MicroChem, Inc.) master, followed by curing at 70 °C for 6 h. The SWNT films and PDMS molds were treated with air plasma (PDC-32G, Harrick Plasma) for 10 s at 6.8 W and for 60 s at 18 W, respectively. After a conformal contact was formed between the plasma-treated SWNT thin film and prepatterned PDMS mold for 10 min, the PDMS mold was removed manually, and high-resolution SWNT electrodes were produced on the hydrophobic HMDS-treated Si/SiO$_2$ substrate. The channel width of the patterned SWNT source−drain electrodes was 800 μm, and the
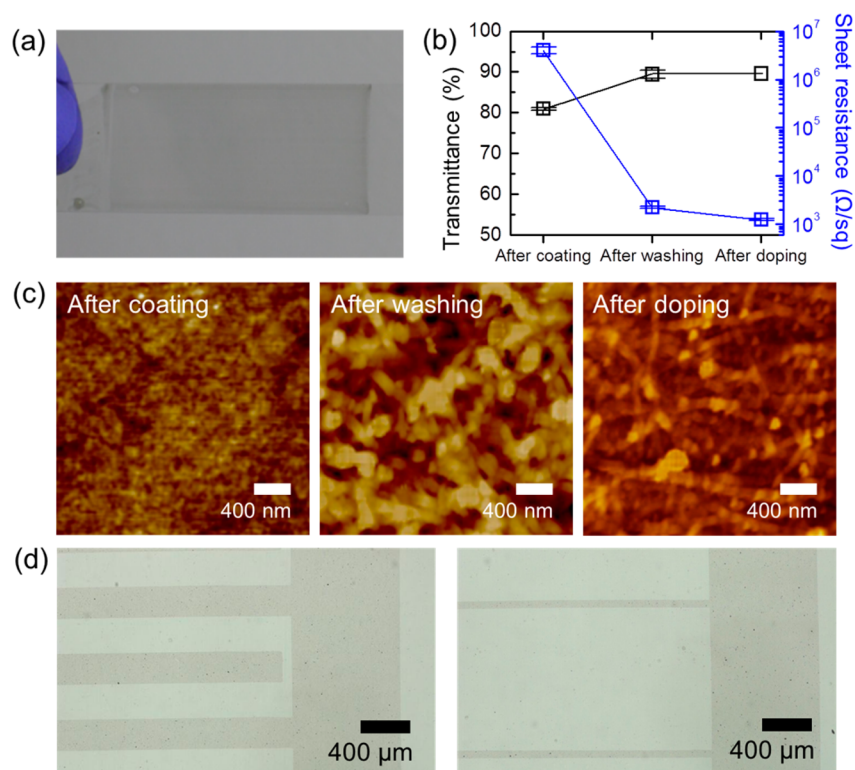
Figure 2. (a) Photograph showing a SWNT thin film coated on a glass slide. (b) Transmittance at λ = 550 nm and sheet resistance of the SWNT thin films after the coating, washing, and doping steps. (c) AFM images of the SWNT thin films after the coating, washing, and doping steps. (d) Optical microscopy images of the SWNT patterns prepared by PEDP.

channel length was varied from 20 to 170 μm. Pentacene and N,N′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8; Aldrich Chemical Co.; no purification) films, 100 nm in thickness, were deposited from a quartz crucible onto the SWNT-patterned substrates at a rate of 0.2 Å s^{-1} using an organic molecular beam deposition system.

Characterization. Optical micrographs of the SWNT micropatterns were acquired by an Olympus BX-51 optical microscope and a high-resolution ProRes CF Scan digital CCD camera (Jenoptik). The morphology of the SWNT micropatterns was obtained using atomic force microscopy (AFM; XE-100, Park Systems). The optical transmittance and sheet resistance of the SWNT thin films were characterized using a UV−vis−near-IR spectrophotometer (Jasco V-670) and a Keithley 2400 instrument, respectively. Ultraviolet photoemission spectroscopy (UPS) was performed by a PHI 5000 VersaProbe with a He I (21.2 eV) source. The current−voltage characteristics of the OFETs were measured at room temperature under vacuum in a dark environment using Keithley 2400 and 236 source/measure units. For the electrical measurements of the devices, the metallic probe was directly contacted on the SWNT electrodes.

3. RESULTS AND DISCUSSION

The procedures used to fabricate the SWNT source−drain electrodes for the bottom-contact and bottom-gate OFETs are illustrated in Figure 1. Highly uniform SWNT thin films were prepared on a hydrophobic HMDS-treated Si/SiO$_2$ substrate using the MDD technique (Figure 1a). As the glass deposition plate was shifted horizontally by a motorized stage, the meniscus of the SWNT suspension trapped between the deposition plate and substrate was drawn, and a thin layer of the SWNT solution was formed behind the entrained meniscus over the coating surface. The SWNTs suspended in the trapped drop were deposited on the substrate by shear force in the thin aqueous layer.[33] The deposition process was repeated during alternating linear-shifting motions of the deposition plate,

leading to the formation of a SWNT network on the HMDS-treated Si/SiO$_2$ substrate. The film was dried at room temperature to provide a uniform large-area SWNT thin film, as shown in Figure 2a. The aqueous dispersion of SWNTs was prepared using a 10 vol % ethylene glycol solution and stabilized by 1 wt % SDBS and 3 wt % TX-100 surfactants. The addition of ethylene glycol was critical for obtaining uniform SWNT thin films. The SWNT-coated films prepared using a SWNT dispersion containing only the aqueous surfactant solution exhibited large defects, contact-line recession, and rupture during the drying process, as shown in Figure S1 in the Supporting Information. Breakage of the thin liquid films was caused by secondary flow due to the dewetting forces and the nonuniform solvent evaporation, which could be avoided by decreasing the surface tension or by increasing the solution viscosity.[9,33] The addition of ethylene glycol to the SWNT coating solution sufficiently increased the viscosity of the SWNT suspension to prevent dewetting of the drying thin films, leading to the preparation of highly uniform SWNT films (Figure 2a). The presence of ethylene glycol improved the dispersion of SWNTs by forming aggregates around the surfaces of the SWNTs in water due to hydrophobic interaction.[34]

After drying, the SWNT thin films were washed by dipping in a 50 vol % ethanol solution at 50 °C for 1 h to remove the surfactants and ethylene glycol from the SWNT surfaces. The films were then completely dried at 80 °C. Although the network of SWNT bundles could not be observed clearly in the AFM images of the as-coated SWNT films, it was clearly visible in the washed SWNT film, as shown in Figure 2c. After the surfactants and ethylene glycol that had been adsorbed onto the SWNT surfaces were washed away, the electrical conductivity
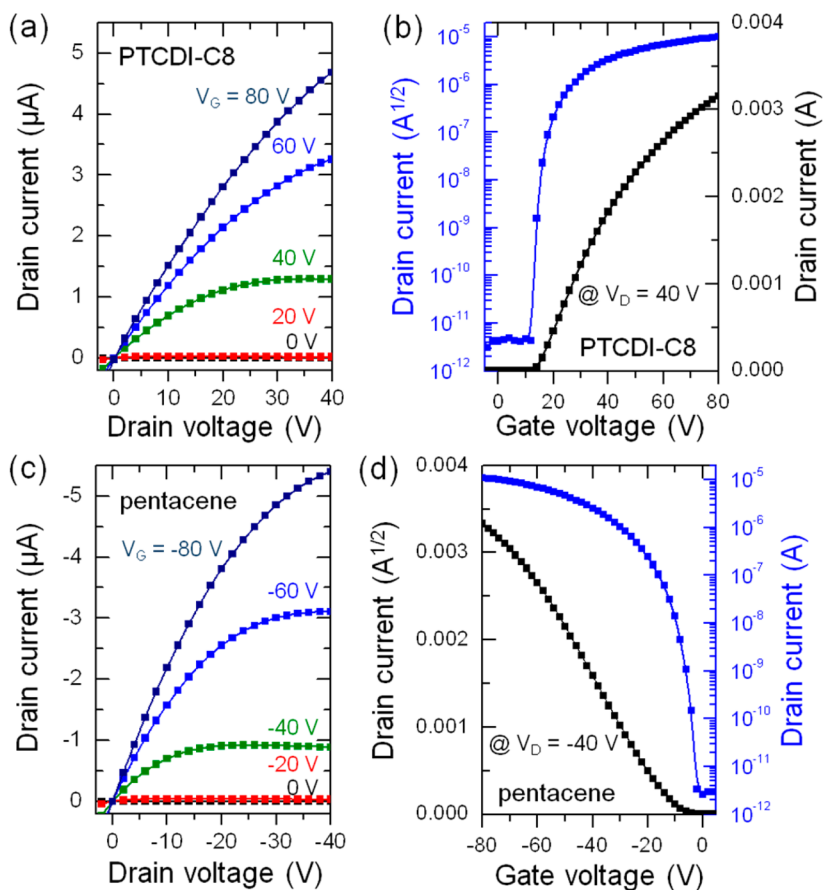
Figure 3. (a) Output characteristics (I_D vs V_D) of the PTCDI-C8 FETs with SWNT electrodes. (b) Transfer characteristics (I_D vs V_G) of the PTCDI-C8 FETs prepared with SWNT electrodes. (c) Output characteristics of the pentacene FETs prepared with SWNT electrodes. (d) Transfer characteristics of the pentacene FETs prepared with SWNT electrodes.

and transparency of the SWNT thin films were significantly enhanced because of better contact between the individual SWNTs (Figure 2b). The electrical properties could be further improved by treating the SWNT thin films with nitric acid. The sheet resistance of the SWNT films was reduced because the acid treatment introduced p doping into the SWNTs by forming charge-transfer complexes and by removing any remaining residual surfactants from the SWNT surfaces (Figures 2b,c and S2 in the Supporting Information).[35−39]

SWNT source−drain electrode patterning for the OFETs was achieved by applying the plasma-enhanced detachment patterning (PEDP) method[40,41] to the MDD-processed SWNT thin films, as shown in Figure 1. Unwanted parts of the SWNT films were delaminated from the substrate as follows. First, both the SWNT thin films formed on the HMDS-treated Si/SiO$_2$ substrate and the prepatterned PDMS molds were treated with air plasma. The PDMS molds were then placed over the SWNT film surface without applying additional pressure or heating. The molds were peeled away from the films to fully detach the SWNTs in contact with the PDMS surface. Finely patterned SWNT electrodes were thereby produced on a hydrophobic Si/SiO$_2$ substrate in a shape defined by the geometry of the mold (Figure 2d). Exposure of both of the SWNT and PDMS surfaces to plasma increased their adhesion to overcome the adhesive forces between the SWNT films and HMDS-treated substrates. The key feature of our coating and patterning method is the ability to form SWNT microstructures based on an aqueous dispersion directly on a hydrophobic substrate,

which is, in general, necessary for achieving high-performance OFETs. Figure S3 in the Supporting Information shows optical microscopy images of typical SWNT source−drain electrode patterns with a channel width of 800 μm and a channel length of 20−170 μm, prepared on the HMDS-treated Si/SiO$_2$ wafer. After the SWNT electrodes formed, the devices were completed by evaporating a 100-nm-thick PTCDI-C8 or pentacene film via thermal evaporation.

The as-prepared SWNT electrodes were first applied to the fabrication of n-type PTCDI-C8 FETs. Figure 3a shows the output characteristics (drain current (I_D) versus drain voltage (V_D) of the PTCDI-C8 FETs prepared with SWNT electrodes having a channel length of 170 μm and a width of 800 μm. The devices were found to operate well as n-type transistors, exhibiting a linear regime followed by a saturation regime with increasing V_D under a constant gate voltage (V_G). Importantly, I_D, at values of V_D that were much smaller than the gate voltage (V_G), exhibited linear behavior, indicating ohmic contact between the PTCDI-C8 films and SWNT electrodes.[42] Figure 3b shows the transfer characteristics (I_D vs V_G) of the PTCDI-C8 FETs prepared with SWNT electrodes at V_D of 40 V. The ON/OFF current ratio of the FETs exceeded 10^6. The threshold voltage (V_{th}) was around 14.1 V. The electron mobility was calculated in the saturation regime (V_D = 40 V) using the relationship $I_D = C_i \mu W (V_G − V_{th})^2 / 2L$, where W and L are the channel width and length, respectively, C_i is the specific capacitance of the gate dielectric (11 nF cm^{-2}), and μ is the electron mobility.[43] The PTCDI-C8 FETs prepared with

SWNT electrodes exhibited an electron mobility of 0.14 cm^2 V^{-1} s^{-1}. The transistor performances measured from more than 10 devices for each electrode are summarized in Table 1.

Table 1. Electrical Properties of the n-Type PTCDI-C8 and p-Type Pentacene FETs Based on SWNT Source−Drain Electrodes Fabricated by PEDP Method

	carrier mobility (cm^2 V^{-1} s^{-1})	ON/OFF current ratio	V_{th} (V)
PTCDI-C8	0.14 (±0.03)	4.3 (±2.8) × 10^6	14.1 (±3.7)
pentacene	0.16 (±0.04)	2.4 (±1.9) × 10^7	−10.8 (±4.5)

The micropatterned SWNT electrodes were used to fabricate p-type pentacene FETs (Figure 3c,d). Similar to the results obtained for the PTCDI-C8 OFETs, the SWNT electrode devices yielded good device performance, such as a high hole mobility of 0.16 cm^2 V^{-1} s^{-1}, a high ON/OFF current ratio exceeding 10^6, and a low threshold voltage of −10.8 V. The hole mobility of the pentacene FETs prepared with SWNT electrodes exactly matched the electron mobility of the PTCDI-C8 FETs prepared with SWNT electrodes, demonstrating excellent compatibility of the as-prepared SWNT electrodes with both n-type PTCDI-C8 and p-type pentacene. Overall, the SWNT electrodes patterned using the PEDP method are applicable to both types of common organic semiconductors and yield OFET performances comparable to those reported previously for OFETs prepared with metal or organic electrodes.[44,45]

The effects of the SWNT contacts on the device performances in PTCDI-C8 and pentacene FETs were quantified from the channel-length-dependent resistance by analyzing the output characteristics at small drain voltages. The contact resistance (R_c) was obtained from the L = 0 intersect of the measured device resistance at each gate voltage, as indicated by the equation[46]

$$R_{total} = R_c + \frac{L}{W[\mu_i C_i (V_G - V_{th,i})]}$$

where μ_i and $V_{th,i}$ are the intrinsic field-effect mobility and threshold voltage, respectively. R_{total} is the total resistance. The channel-width-normalized total resistances of the PTCDI-C8 and pentacene FETs prepared with SWNT electrodes were plotted as a function of the channel length for each V_G, as

shown in parts a and b of Figure 4, respectively. The y intercept of the $R_{total}W$ versus L plot was used to evaluate the contact resistance as a function of the gate voltage. The channel-width-normalized $R_{contact}$ decreased from 0.90 to 0.06 MΩ cm for the PTCDI-C8 FETs and from 0.66 to 0.03 MΩ cm for the pentacene FETs as |V_G| was varied from 20 to 80 V (Figure 4c). The well-matched contact resistances from two different systems probably arose from similar charge-injection barrier heights for the respective charge carriers at the electrode/semiconductor junctions.[47] The work function of our SWNT electrodes was estimated to be 4.7 eV based on UPS measurements. This work function was intermediate between the LUMO level of PTCDI-C8 (4.3 eV) and the HOMO level of pentacene (5.0 eV). Accordingly, one would expect that the electron-injection barrier at the PTCDI-C8/SWNT electrode interface would be equivalent to the hole-injection barrier at the pentacene/SWNT electrode interface, leading to well-matched electrical properties for the n-type PTCDI-C8 and p-type pentacene FETs.

Finally, the SWNT electrodes fabricated using the PEDP method were successfully applied to the fabrication of a complementary logic inverter, as shown in Figure 5a. A complementary inverter was fabricated by connecting a p-type pentacene FET to an n-type PTCDI-C8 FET. The comparable electrical performances of the n- and p-type FETs paired with the SWNT electrodes (equivalent current level at given values of V_G and V_D) facilitated the fabrication of complementary circuits because of the use of a single electrode in both transistors. The complementary inverters exhibited good voltage-transfer characteristics, as shown in the left panel of Figure 5b. As the supply voltage (V_{DD}) increased from 40 to 80 V, the output voltage (V_{OUT}) remained comparable to the V_{DD} values at low input voltages (V_{IN}) and was 0 V at high V_{IN}. This indicated that the p- and n-type FETs turned on and off, respectively, at low values of V_{IN} and vice versa at high V_{IN}.[48] The complementary inverter functioned well over the range of V_{DD} tested. The signal inverter gain, defined as the absolute value of dV_{OUT}/dV_{IN}, is shown in the right panel of Figure 5b as a function of V_{DD}, with a maximum value of 17.0 at V_{DD} = 80 V. For comparison, the inverter devices prepared with single gold electrodes were also fabricated. The devices exhibited much lower gain values of 10.4 at V_{DD} = 80 V, possibly due to the mismatch between the hole and electron current levels of the pentacene and PTCDI-C8 FETs, respectively (Figure S4 in
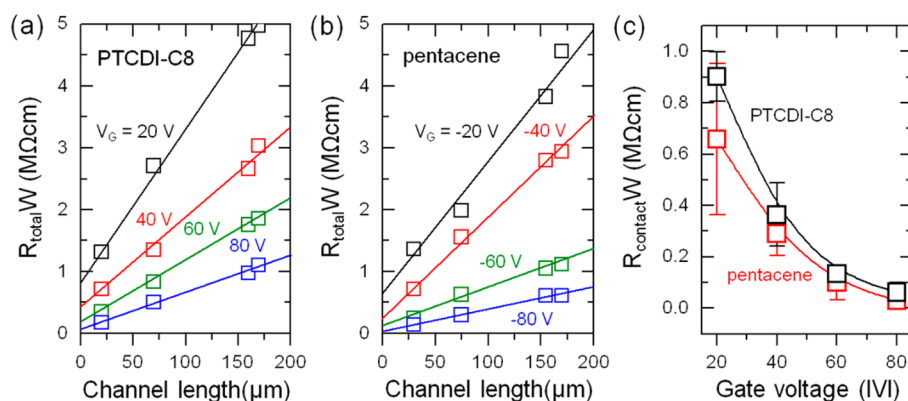

Figure 4. Channel-width-normalized R_{total} as a function of the channel length at gate voltages between 20 and 80 V, collected at 20 V intervals, of the PTCDI-C8 (a) and pentacene (b) FETs based on SWNT source−drain contacts. (c) Channel-width-normalized $R_{contact}$ as a function of the gate voltage.
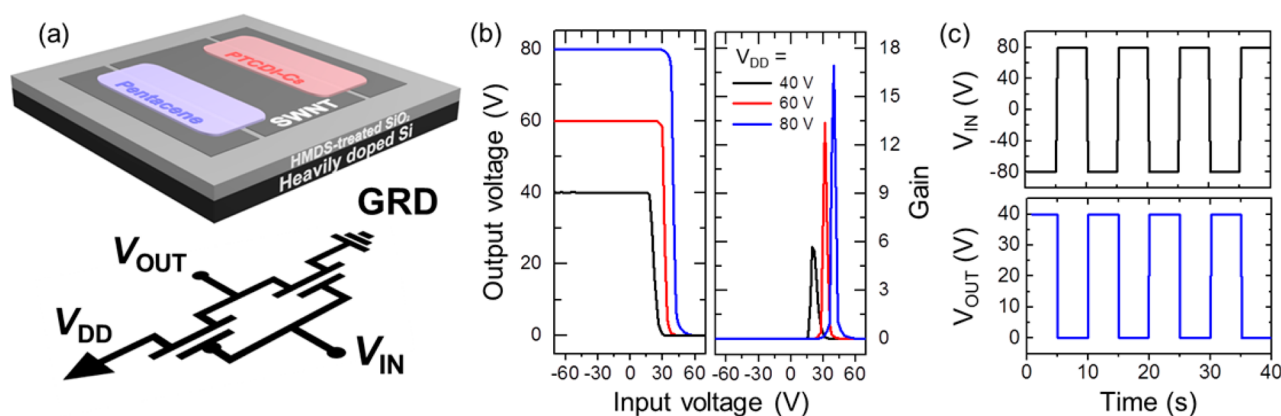
Figure 5. (a) Schematic diagram and electrical connection setup of a complementary inverter based on the n-type PTCDI-C8 and p-type pentacene FETs fabricated on plastic. (b) Voltage transfer characteristics (left panel) of the complementary inverter under various V_{DD} values and their corresponding signal gain (right panel). (c) Output voltage response of the complementary inverter prepared with SWNT electrodes at V_{DD} = 40 V for V_G pulsed at 0.1 Hz.

the Supporting Information). The dynamic response characteristics of the inverter output signal were characterized under V_{DD} = 40 V, as shown in Figure 5c. The output voltage of the inverter responded well to a square-wave input voltage signal.

4. CONCLUSIONS

In conclusion, we developed a reproducible and effective method for preparing uniform SWNT thin-film coatings and for patterning highly defined SWNT electrode arrays on hydrophobic substrates for use in bottom-contact n-type and p-type OFETs. The uniform SWNT electrode patterns prepared on a hydrophobic silanized SiO_2 wafer were successfully prepared by engineering the surface energy with the assistance of oxygen plasma. Both n-type PTCDI-C8 and p-type pentacene FETs based on the patterned SWNT electrodes exhibited high and exactly matched field-effect mobilities. A high-performance complementary inverter was successfully fabricated using a single SWNT electrode material. The proposed technique for preparing micropatterned SWNT coatings was easy and scalable and offered significant promise for the preparation of next-generation flexible electronics.

ASSOCIATED CONTENT

Ⓢ Supporting Information

Optical micrograph, optical micrograph and SEM images, and voltage transfer characteristics. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes
The authors declare no competing financial interest.

ACKNOWLEDGMENTS

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